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Title:

SYSTEMS AND METHODS FOR PROVIDING DISTRIBUTED CONTROL SIGNAL REDUNDANCY AMONG ELECTRONIC CIRCUITS

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SYSTEMS AND METHODS FOR PROVIDING DISTRIBUTED CONTROL SIGNAL REDUNDANCY AMONG ELECTRONIC CIRCUITS

FIELD OF THE INVENTION

[0001] This invention relates to the provision of inter-circuit control signals and more particularly to systems and methods for providing distributed control signal redundancy among electronic circuits.

DESCRIPTION OF RELATED ART

[0002] In multiple-circuit electronic systems it is often necessary to send control signals, such as, for example, clock signals, to control system timing among the various physically separated circuits. These circuits are usually contained on separate electronic boards all in electronic communication. In many situations, it is desirable that timing signals from a single clock control the circuitry on all of the boards. This, then, argues for a single clock source positioned physically on one of the boards (the clock-control board) with these signals then interconnected, by a signal transmission system, such as a cable, to all of the other boards.

[0003] For reliability, it has become common practice to provide dual redundancy for these clock signals. Thus, two clocks are typically provided on the clock control board and two cables are provided among the boards. Thus, if a clock fails, a second clock is available to provide the timing signals. If one of the signal transmission cables fails, then the other transmission cable distributes the clock signals from the clock board.

[0004] However, if the power to the clock board fails (a single failure) both clocks on that board fail causing, in effect, a dual failure. Thus, a single failure effectively brings down the entire system. Also, when one of the clocks fails, the system is thereafter vulnerable to a single clock failure until the failed clock is replaced. Replacing the failed clock without removing the clock board, or at least without removing the power to the clock board, is not usually possible.

BRIEF SUMMARY OF THE INVENTION

[0005] In one embodiment, a distributed redundant control signal distribution system comprises a first control signal source co-located with a first set of control signal

controlled circuit elements, at least one second control signal source co-located with a second set of control signal controlled circuit elements, at least one controller for providing control signals from the first control signal source to control both the first and second sets of controlled circuit elements, the controller operable for substituting signals from the second control signal source for signals from the first signal control source if the signals from the first control signal source become unavailable to either the first or second circuit elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIGURE 1 shows one embodiment of a dual backplane system having redundant control signals;

[0007] FIGURES 2, 3 and 4 show the embodiment of FIGURE 1 in various failure modes;

[0008] FIGURE 5 shows an embodiment of a system having multiple backplanes with two separate control signal sources; and

[0009] FIGURE 6 shows a flow chart of one embodiment for selecting the proper control signal.

DETAILED DESCRIPTION

[0010] Referring now to FIGURE 1, system 10 is one embodiment of a dual backplane or system having multiple control signal sources. In the embodiment shown, the control signals are from primary clock source 11 and secondary clock source 12. The secondary clock source is on a board (or backplane) different from the primary clock source. Backplane 0 (BP0) has four input multiplexer 13-0 that operates under control of control circuit 17-0 to switch one of the inputs A, B, C, D to the output of mux 13-0 following an established procedure as will be discussed. The clock output from mux 13-0 is provided to circuitry 16-01 to 16-0N co-located on backplane BP0. The same clock output of mux 13-0 is provided via amplifiers 14-0 and 15-0 over dual cable 101 to the inputs B and C of mux 13-1 located on backplane 1 (BP1).

[0011] Note that the transmission path may be cables or could be wireless, microwave, etc. Backplane BP1 is constructed almost exactly as is backplane BP0, except that

secondary clock source 12 is connected to the D input of mux 13-1 instead of to the A input as was primary clock source 11 in backplane BP0. Control 17-0 (and control 17-1) receive primary and secondary clock signals as shown. Since there is no A input to mux 13-1. The B input from cable 101 is switched to the mux output and to control signal controlled circuits 16-11 to 16-1N. These same signals (the primary clock signal from board BP0) is fed back via cable 102 to the B and C inputs to mux 13-0. This has no effect on the system, since mux 13-0, under control of control 17-0 continues to have the A input (primary signal source) switched to the output of mux 13-0.

[0012] One embodiment 60 utilized by processors 17-01 and 17-11 in control circuits 17-0 and 17-1 for controlling mux 13-0 and 13-1 is shown in FIGURE 6. Essentially mux 13-0 takes the inputs in hierarchical order A, B, C and D such that if a signal is present on input A then the A input will be provided to the mux output. Absent a signal on input A, the mux looks for signals on B, C and D in that hierarchical order. As shown in FIGURE 6, this operation is controlled by process 601, such that so long as a valid signal is received from the primary clock source, the mux is controlled by process 602 to follow the hierarchical order A, B, C and D. This procedure is followed in all backplanes (boards) having a clock source.

[0013] If the primary clock source fails (or is not valid) then process 603 determines if the secondary clock source is valid. If the secondary clock source is valid, then the hierarchical order is D, C, B, A. Again, this procedure is followed in all backplanes (boards) having a clock.

[0014] Turning now to FIGURE 2, and assuming that a default occurs on the B portion of transmission path 101. When that occurs, there is no signal on the B input of mux 13-1. Mux 13-1 then switches to its C input. Since the C input also contains signals from primary clocks source 11 the output of mux 13-1 continues to provide control of the circuit elements on backplane BP1 from the primary clock source on board BP0.

[0015] As shown in FIGURE 3, in the event that primary clock source 11 were to fail, then the signal from primary clock source 11 is removed from the output of mux 13-0 and thus removed from both paths of transmission paths 101 and also from the B and C inputs of mux 13-1. In this situation, signals from secondary clock source 12 are switched from the D input of mux 13-1 to its output. Accordingly, the signals from secondary clock source 12 drives

the circuits co-located on backplane BP1. This signal is provided to amplifiers 14-1 and 15-1 and over transmission path 102 to the B and C inputs of mux 13-0. Mux 13-0 then switches the secondary clock signals to its output to control the circuits on board BP0.

[0016] As discussed above, and as shown on FIGURE 6, since the primary clock signals are not valid, both mux 13-0 and 13-1 switch to the D, C, B, A hierarchy. This has no effect on board BP0, but on the board BP1 it has the effect of preventing an unstable condition as mux 13-1 otherwise would switch back and forth between input D and B. This would occur because the secondary clock signal is fed back over transmission path 101 and would appear on the B and C inputs of mux 13-1. Thus, unless process 60, or a similar process were to be used, the signal on the B (or C) input of mux 13-1 would cause the mux to switch to the signal on the B (or C) input. If this were to occur, then the signal from clock source 12 (on input D) would cease to be the output of mux 13-1 and the system could go into oscillation.

[0017] Turning now to FIGURE 4, if both paths of transmission path 101 are faulted then this would be a double fault condition and since the system is designed to protect against single faults, the system would go into asynchronous operation with secondary clock source 12 driving the elements co-located on backplane BP1 and primary clock source 11 driving the circuit elements co-located therewith on backplane BP0.

[0018] The system could be designed having more paths interconnecting the various backplanes (and move mux inputs) thereby providing higher redundancy levels if desired.

[0019] Turning now to FIGURE 5, there is shown an embodiment 50 of a multi backplane system having two clock sources and several backplanes, such as backplanes BP0 through BPN. The embodiment shown in system 50 works the same as discussed with respect to the embodiment shown in FIGURE 1, except that, backplanes BP2 through BPN do not have clocks local thereto. Although, the system could have as many clocks as desired. In the embodiment shown, backplanes BP2 through BPN will have the same clock as all the other boards via cables 501 and 503.